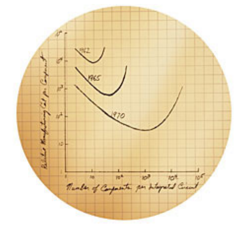


An Outlook of Technology Scaling Beyond Moore's Law

Adrian M. Ionescu
Ecole Polytechnique Fédérale de Lausanne

Summary

- **Introduction**: Moore's law…
- **More Moore, Beyond CMOS, More-than-More**
- **Fundamental limits**
- **Evolutionary and non-classical MOSFET (More Moore…)**
- **Emerging nanoelectronics (… beyond CMOS)**
  - Single/few electron electronics & QCA
  - Nanowires & carbon nanotubes
  - Molecular electronics
  - Spintronics
- **Conclusion**

40 years of Moore's law: 1965 - 2005

- 1965: **a single transistor cost more than a dollar**
- 1975: the cost of a transistor had dropped to less than a penny, while transistor size allowed for almost 100,000 transistors on a single die
- 1979 to 1999, processor performance went from about 1.5 million instructions per second (MIPS), to almost 50 MIPS on the i486™, to over 1,000 MIPS on the Intel® Pentium® III
- Today's Intel® processors run at 3.2 GHz and higher, deliver over 10,000 MIPS, and can be manufactured in high volumes with **transistors that cost less than 1/10,000th of a cent**

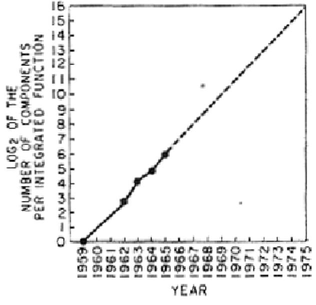
How it started…

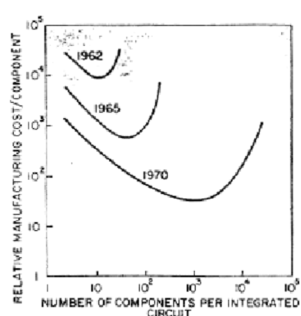
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

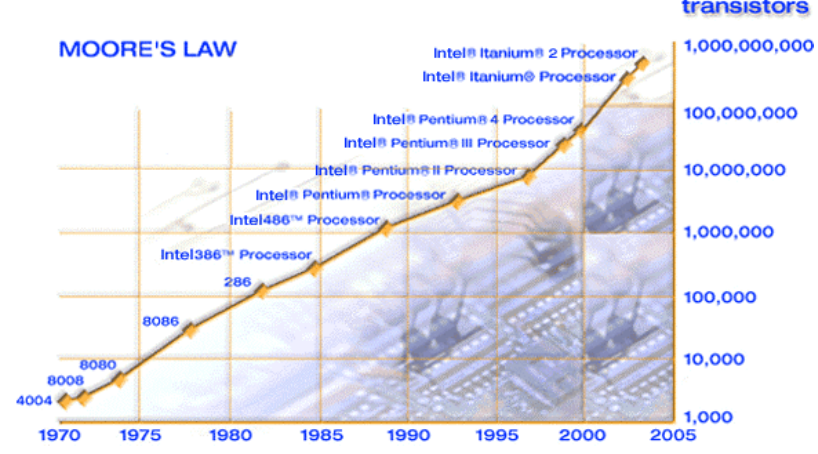
By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.



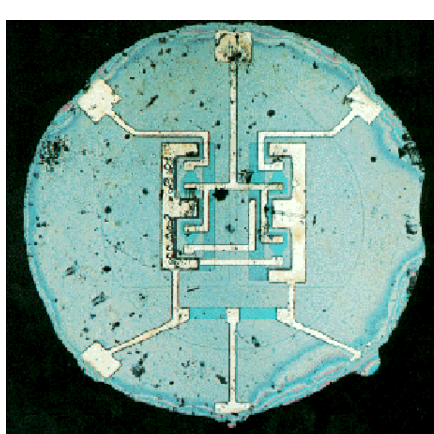


… and where we are…

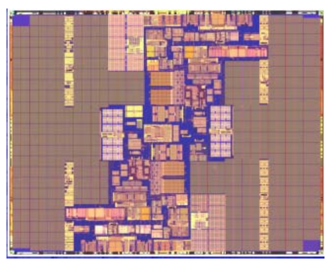


Source: http://www.intel.com/research/silicon/mooreslaw.htm

First planar integrated circuit (1961)

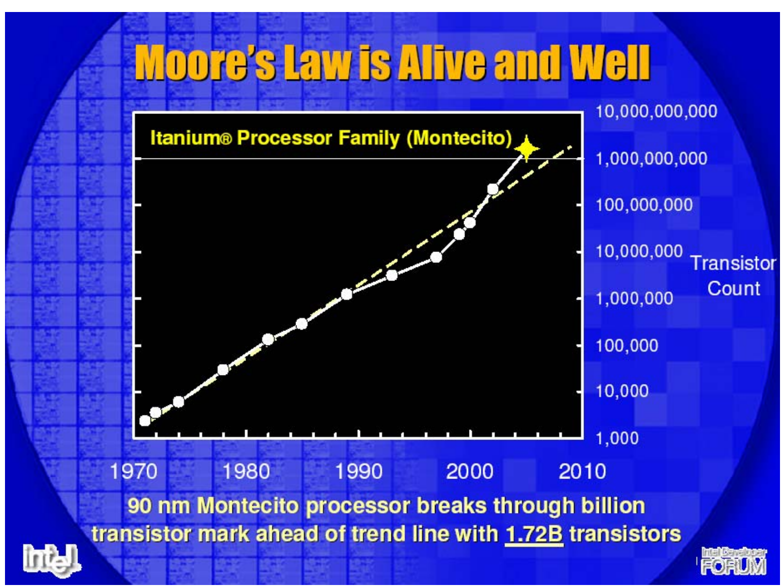


90 nm Intel's processor Montecito (2004) Itanium Processor Family



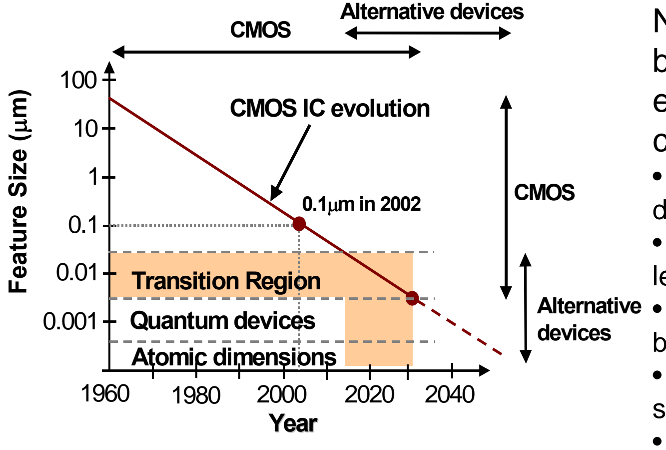
Transistors: 1.72 Billion
Frequency: >1.7GHz
Power: ~100W

Source: Intel Developer Forum, September, 2004



Source: M. Bohr, Intel Development Forum, September 2004.

CMOS scaling (1)

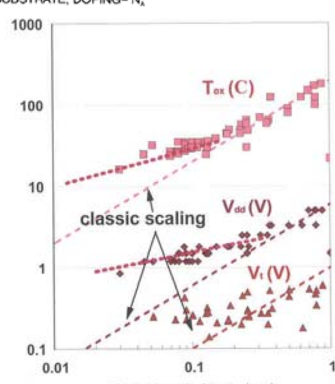


Nanotechnology benefits for electronics and computing:

- nano-processors with declining energy
- ultra-small terra-bit level storage
- > GHz frequency and bandwidth
- integrated nano-sensors
- novel functionalities

CMOS scaling (2)

Classical Scaling (Denard)		Consequence	
Voltage:	V/α	Higher density:	α^2
Oxide:	t_{ox}/α	Higher speed:	α
Wide width:	W/α	Power:	$1/\alpha^2$
Gate width:	L/α	Power density:	const.
Diffusion:	x_d/α		
Doping:	αN_A		

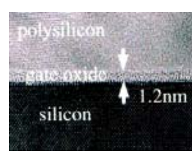


Deviations from classical scaling
- gate leakage
- reliability
- performance at higher voltage

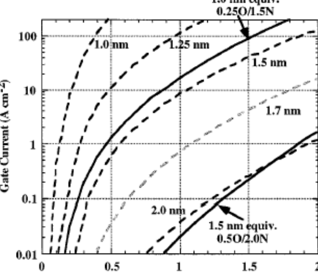
Consequence
- **increase of power density**

Adapted after: H-S. P. Wong, et al., Proceedings of the IEEE, vol. 87, No. 4, pp. 537-70, 2001.

Gate dielectric @ fundamental scaling limit



Practical limits on the thickness of the SiO_2 gate oxide are crucial. Two fundamental considerations:
- **roughness to be controlled** @ atomic scale: leakage of 1nm oxide increases by 10 every 0.1nm rms roughness
- **intrinsic transition region** to reach bulk SiO2 properties: **0.3-0.5 nm**

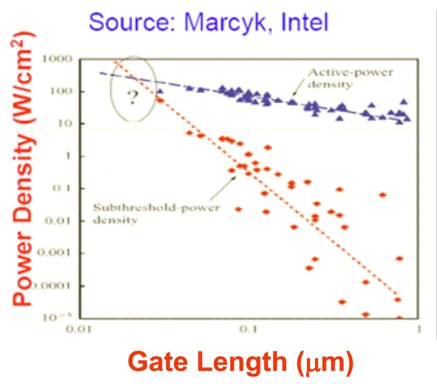


Assume tolerable gate leakage is 100 Acm and gate area is 1% of a 1-cm chip and power-supply voltage of 1 V, the power dissipation due to the gate current is 1 W.

J. D. Plummer and P. B. Griffin, Proceedings of the IEEE, Vol. 89, pp. 240 –258, 2001.
D. A. Muller et al., Nature, pp. 758-761, June 1999.

Power is key limiting factor?

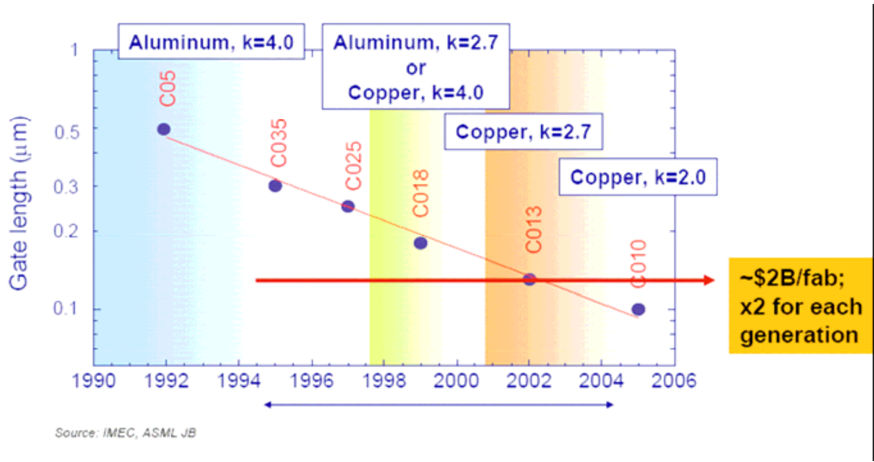
- Active power
- Passive power (gate & subthreshold leakage)



Problems:

- Server microprocessors cannot simultaneaously use all their transistors due to power limitations
- Leakage power limits max usable μP frequency

Cost limit



Fundamental limits

From: **thermodinamics, quantum-mechanics, electromagnetics**

- Limit on energy transfer during a binary switching:
  E(min) = (ln2) kT (=kTlog$_e$N, N=2) (J. Neumann)
- Heisenberg's uncertainty principle:
  ΔE > h/Δt → forbidden region for power-delay
- electromagnetics → **τ > L/c_0** (limited time of electromagnetic wave travelling across interconnects)

Why E(min) = kT x ln2 ?

Binary signal discrimination: the slope of the static transfer curve of a (CMOS) binary logic gate must be greater than unity in absolute value at the transition point where input and output voltage levels are equal → **CMOS inverter**

$$\mathrm{Vdd(min)} = 2[kT/q]\left[1+\frac{C_{fs}}{C_{ox}+C_d}\right]\ln(2+\frac{C_d}{C_{ox}})$$

$$\mathrm{Vdd(min)} \cong 2(\ln 2)\frac{kT}{q} = 1.38\frac{kT}{q} = 0.036\mathrm{V}\ @\ T = 300\mathrm{K}$$

Min signal energy stored on gate:

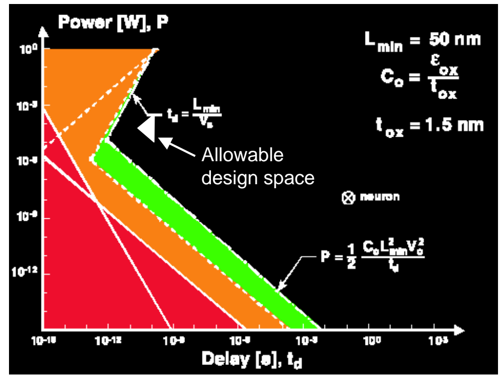
$$\mathrm{Es(min)} = (1/2)Q_g\mathrm{Vdd} = (1/2)q\ \mathrm{x}\ 2(\ln 2)\frac{kT}{q} = kT\ \mathrm{x}\ \ln 2 == 0.693kT$$

$$\mathrm{with:}\ C_g = \frac{\varepsilon_{ox}L^2_{min}}{t_{ox}} \Rightarrow\ L_{min} = \left[\frac{t_{ox}}{\varepsilon_{ox}}\right]q^2/[2(\ln 2)kT]^{1/2} = 9.3\mathrm{nm}\ @\ t_{ox} = 1\mathrm{nm}$$

Source: J.D. Meindl, J. A. Davis, IEEE JSSC, Vol. 35, October 2000, pp. 1515-1516.

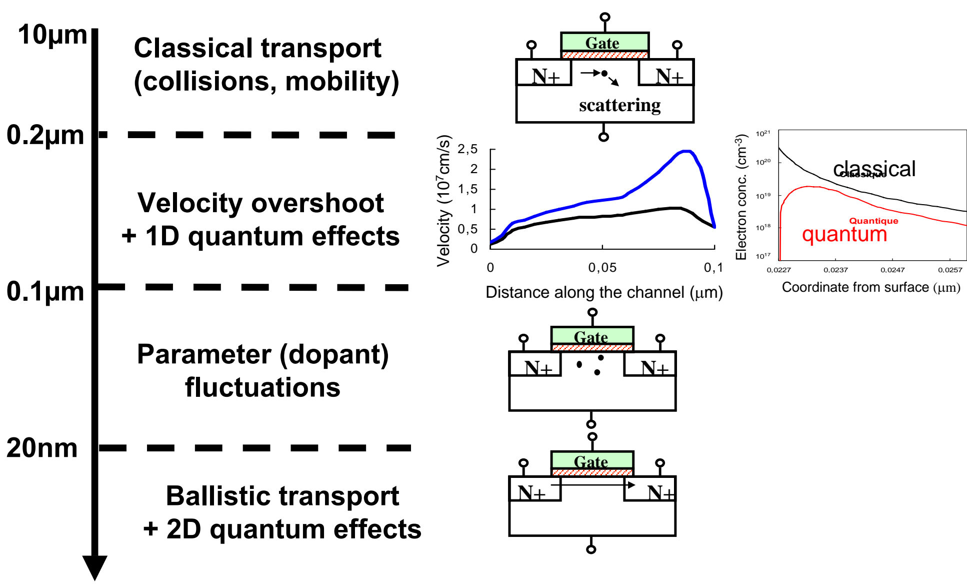
Fundamental limits

Average power transfer during a binary transition, *P*, versus transition time, *t*d. The red, orange, and green zones are forbidden by fundamental, silicon material, and 50-nm channel length transistor device level limits,respectively.



Source:
J. D. Meindl, Q. Chen, J. A. Davis, Science, Vol. 293, pp. 2044-2049, September 2001

MOSFET @ nanoscale: what changes?



Example: Process Variations (1)

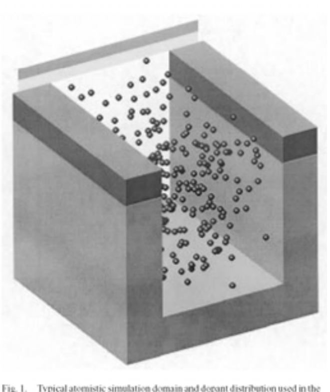


Fig. 1. Typical atomistic simulation domain and dopant distribution used in the simulation of a 30 × 50 nm n-channel MOSFET with oxide thickness $t_{ox} = 3$ nm, junction depth $x_j = 7$ nm, and channel acceptor concentration $N_A = 5 \times 10^{18}$ cm^{-3}.

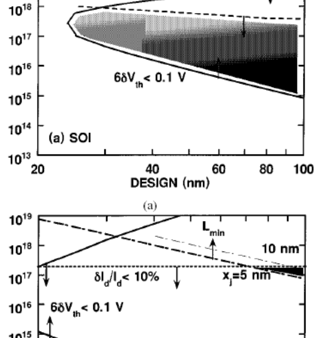
- **main affected parameter: V_T**
- both the **discrete random dopant distribution** in the channel region and the **quantum effects in the inversion layer** should be considered for < 100nm
- due to **channel dopant variations** in individual devices, **threshold voltage fluctuations in ULSI's are estimated to exceed 0.1 V in the for less than 0.1 μm** if the doping is not optimized

Source:
T. Mizuno, IEEE Transactions on Electron Devices, Vol. 47, pp. 756–761, April 2000.
A. Asenov et al., IEEE Transactions on Electron Devices, Vol. 48, pp. 722-729, April 2001.

Example: Process Variations (2)

There is a <u>most suitable</u> N_A to supress δVT

- **SOI:** $N_0 = \frac{kT}{q^2}\frac{C_{ox}}{T_{SOI}}$
- **bulk-Si:** $N_0 = \left(\frac{kT}{q}\right)^2 \frac{C_{ox}^2}{q\epsilon_s\phi_B} = 1.5 \times 10^{16}\ \text{cm}^{-3}$

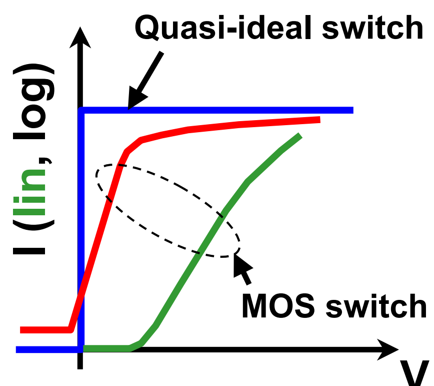


Design for N_A vs Leff in nano-region ULSI:
(a) SOI
(b) bulk MOSFET's.
The shaded regions indicate suitable N_A for $\Delta I / I < 10\%$, $6\delta V < 0.1$ V, and suppressing the short channel effects.

More design space exists for SOI!

The ideal MOS switch @ nanoscale: what should be improved?

- Control of short channel effects → V_T, Ioff
- Subthreshold slope: **better than 60mV/decade?**
- Mobility, velocity saturation, ballistic transport → **Ion**
- Contact and series resistances
- Impact of process variations



Solutions for better-than-60mV/decade subthreshold slope

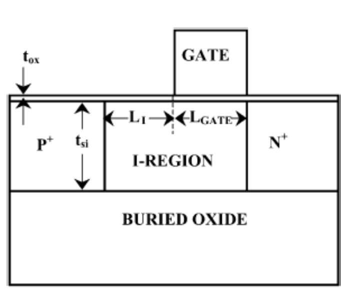
$$S = \ln 10 \frac{kT}{q}\left(1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{ss}}{C_{ox}}\right) \rightarrow \frac{kT}{q}\ln 10 = 60\text{mV/decade}$$

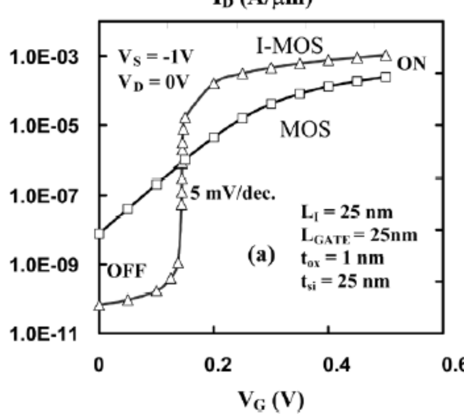
Various concepts:

- I-MOS
- Tunnel FET
- NEM-MOSFET
- Hybrid devices
- …

I-MOS

Subthreshold slope improvement by avalanche breakdown current in gated-diode





Source: K. Gopalakrishnan et al., IEEE Transactions on Electron Devices, Vol. 52, Jan. 2005 pp. 69 – 76.

Si/SiGe Vertical Tunnel FET (1)

- Why S < 60mV/decade in tunnel FET?

$$I = AV_{eff}\xi \cdot \exp(-\frac{B}{\xi})$$

$$S = (d\log I_d / dV_{gs})^{-1}$$ **< 60mV/dec**

$$= \ln 10(\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{\xi + B}{\xi^2}\frac{d\xi}{dV_{gs}})^{-1}$$

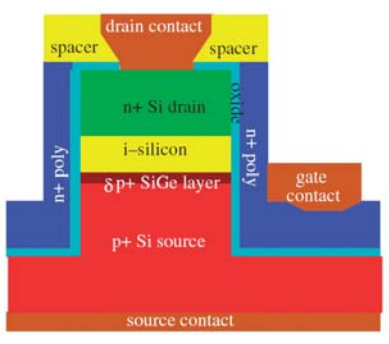
< 60mV/dec / ln10 = 26mV/dec

$$S = \frac{V_{GS}^2}{2V_{GS} + B_{Kane}E_g^{3/2} / D}$$

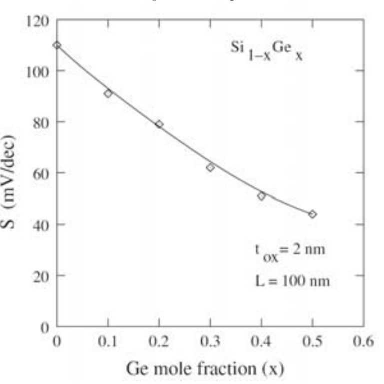
Where:

- Bkane depends on effective mass
- D depends on tox, L, Vds, and dopings

Si/SiGe Vertical Tunnel FET (2)

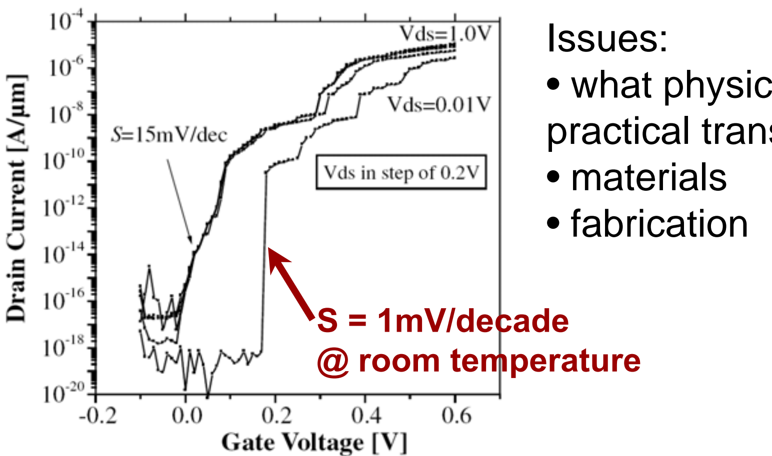


Subthreshold swing S vs. Ge mole fraction in the δp^+ layer



Source:
K. K. Bhuwalka, J Schulze and I Eisele, J. J. of Appl Phys 43, 4073 (2004)

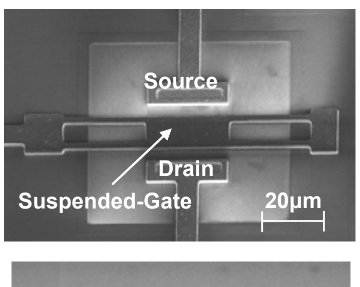
Simulation prediction: SS of tunnel FET

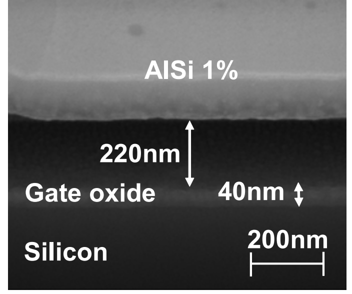


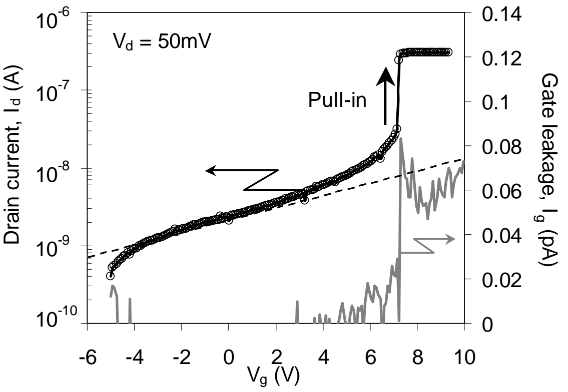
Issues:
- what physics and practical transistor
- materials
- fabrication

Source : P. F. Wang et al. Solid-State Electronics 48, 2281 (2004).

NEM or Suspended-Gate FET

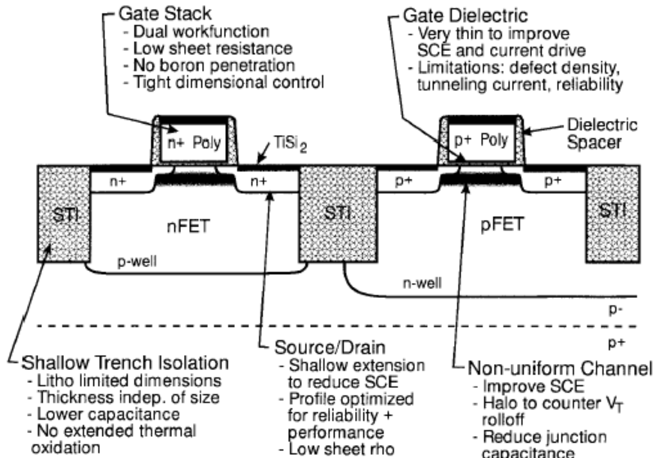






- ultra-low gate leakage in off-state (quasi-negligible)
- 10mV/decade SS demonstrated by EPFL

Evolutionary MOSFET: more Moore…



Source: H-S. P. Wong, et al., Proceedings of the IEEE, vol. 87, No. 4, pp. 537-70, 2001.

Non-classical MOSFET (1): more Moore…

Table 59a Single-gate Non-classical CMOS Technologies

Device	*Transport-enhanced FETs*	*Ultra-thin Body SOI FETs*		*Source/Drain Engineered FETs*	
	Strained Si, Ge, SiGe; buried oxide; Silicon Substrate	BOX	FD Si film; S; D; Ground Plane; BOX (<20nm); Bulk wafer	silicide; nFET; pFET; Schottky barrier isolation	S; D; Non-overlapped region
Concept	Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI	Fully depleted SOI with body thinner than 10 nm	Ultra-thin channel and localized ultra-thin BOX	Schottky source/drain	Non-overlapped S/D extensions on bulk, SOI, or DG devices
Application/Driver	HP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP CMOS	HP, LOP, and LSTP CMOS
Advantages	▪ High mobility	▪ Improved subthreshold slope ▪ No floating body ▪ Potentially lower E_{eff}	▪ SOI-like structure on bulk ▪ Shallow junction by geometry ▪ Junction silicidation as on bulk ▪ Improved S-slope and SCE	▪ Low source/drain resistance	▪ Reduced SCE and DIBL ▪ Reduced parasitic gate capacitance

Non-classical MOSFET (2): more Moore…

Table 59b Multiple-gate Non-classical CMOS Technologies

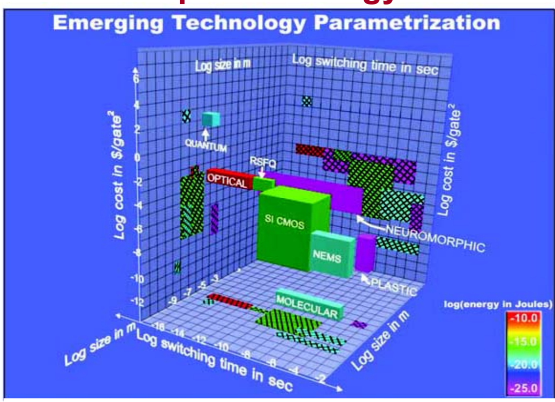
Device	*Multiple Gate FETs*				
	N-Gate (N>2) FETs	*Double-gate FETs*			
		Gate; Source; Drain	SOURCE; GATE; DRAIN; Si-substrate; STI		Gate Gate; Drain
Concept	Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction
Application/ Driver	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	LOP and LSTP CMOS	HP, LOP, and LSTP CMOS
Advantages	▪ Higher drive current ▪ 2× thicker fin allowed	▪ Higher drive current ▪ Improved subthreshold slope ▪ Improved short channel effect	▪ Higher drive current ▪ Improved subthreshold slope ▪ Improved short channel effect	▪ Improved short channel effect	▪ Potential for 3D integration
Particular Strength	▪ Thicker Si body possible	▪ Relatively easy process integration	▪ Process compatible with bulk and on bulk wafers ▪ Very good control of silicon film thickness	▪ Electrically (statically or dynamically) adjustable threshold voltage	▪ Lithography independent L_g
Potential weakness	▪ Limited device width ▪ Corner effect	▪ Fin thickness less than the gate length ▪ Fin shape and aspect ratio	▪ Width limited to <1 μm	▪ Difficult integration ▪ Back-gate capacitance ▪ Degraded subthreshold slope	▪ Junction profiling difficult ▪ Process integration difficult ▪ Parasitic capacitance ▪ Single gate length

Emerging (nano)technologies

No mature and/or credible candidate for ‘beyond CMOS’ yet!

4-D parametrization of emerging nano-technologies:

size x speed x energy x cost



Source:
J. A. Hutchby et al., IEEE Circuits and Devices Magazine, Vol. 18, pp. 28–41, March 2002.

Emerging logic devices (…after Moore)

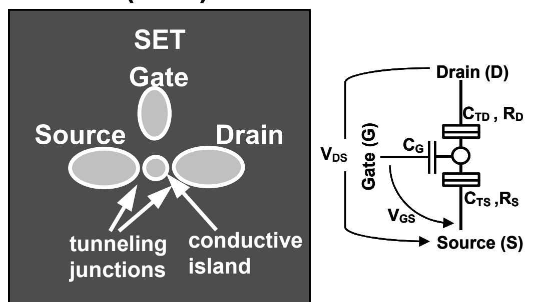
Table 4. Emerging Logic Devices

DEVICE	RESONANT TUNNELING DIODE - FET	SINGLE ELECTRON TRANSISTOR	RAPID SINGLE QUANTUM FLUX LOGIC	QUANTUM CELLULAR AUTOMATA	NANOTUBE DEVICES	MOLECULAR DEVICES
TYPES	3-Terminal	3-Terminal	Josephson Junction +Inductance Loop	-Electronic QCA -Magnetic QCA	FET	2-Terminal and 3-Terminal
ADVANTAGES	Density, Performance, RF	Density, Power, Function	High Speed, Potentially Robust, (Insenstive to Timing Error)	High Functional Density, No Interconnect in Signal Path, Fast and Low Power	Density, Power	Identity of Individual Switches (e.g., Size, Properties on Sub-nm Level. Potential Solution to Interconnect Problem
CHALLENGES	Matching of Device Properties Across Wafer	New Device and System, Dimensional Control (e.g., Room Temp Operation), Noise (Offset Charge), Lack of Drive Current	Low Temperatures, Fabrication of Complex, Dense Circuity	Limited Fan Out, Dimensional Control (Room Temperature Operation), Architecture, Feedback from Devices, Background Charge	New Device and System, Difficult Route for Fabricating Complex Circuitry	Thermal and Environmental Stability, Two Terminal Devices, Need for New Architectures
MATURITY	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated

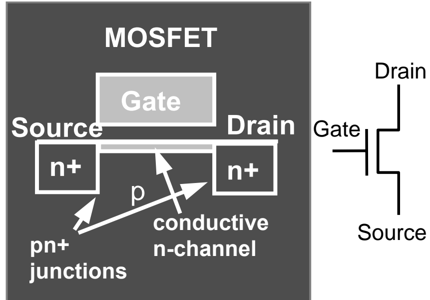
Source: ITRS 2003.

Single/few electron electronics

Single Electron Transistor (SET) *versus* MOS transistor (MOSFET)



- electron conduction is one by one (!)
- drain & gate control Coulomb blockade (CB)
- needs opaque junctions: $R_T > R_Q \sim 26k\Omega$
- needs very small island (~1nm) for room temperature operation



- many electrons simultaneously participate to the conduction
- gate controls channel
- junctions highly transparent
- works inherently at room temperature

HOW SET works?

- SET principle (orthodox theory): K.K. Likharev, 1985
- SET first experimental validation: Fulton & Dolan, 1986

Orthodox theory of Single Electron Transistor

- **Tunnel resistance is much higher than quantum resistance:** $R_{TD,S} >> R_Q = h/e^2 = 25.8k\Omega$
- **Quantization of energy is neglected :** $E_K << k_BT$ ou $E_K << E_C$
- **Tunneling time is neglected: ~10^{-14} - 10^{-15} s**
- **Co-tunneling (multiple) is neglected**

$$\Delta E \times \Delta t \geq h \rightarrow \frac{e^2}{C} \times R_T C \geq h$$

$$R_T \geq R_Q = \frac{h}{e^2} \cong 25.8k\Omega$$

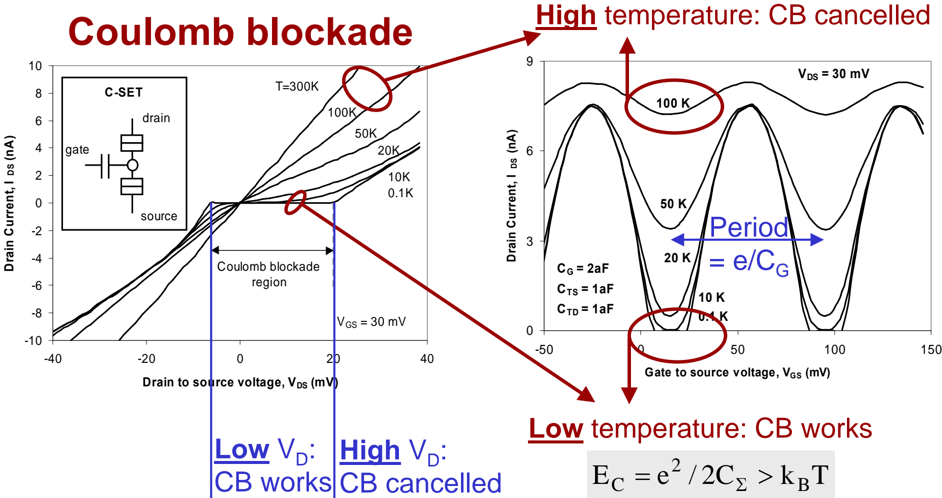
R_Q is not 'real' but a quantum phenomenological resistance

SET is not a real quantum device: charge discrete, energy & current not

SET basic & unique characteristics

Coulomb blockade

High temperature: CB cancelled



Low temperature: CB works

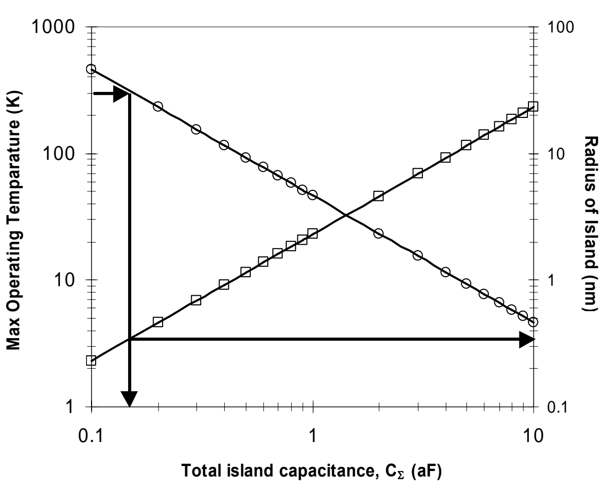
Low V_D: CB works | **High** V_D: CB cancelled

$$E_C = e^2/2C_\Sigma > k_B T$$

Remark: SET has two threshold voltages in terms of both V_G and V_D!

SET room temperature operation

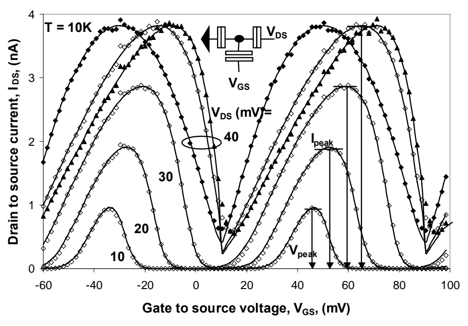
Huge technology challenge: sub-1nm dot size for operation @ T~300K

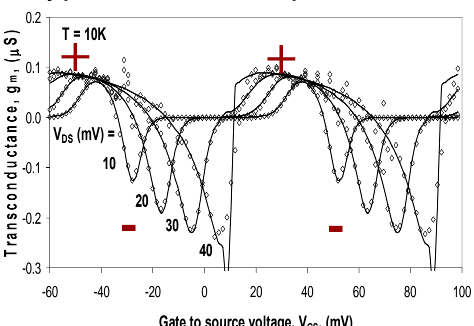


Assymetric SET: unique features

I_{DS}-V_{GS}, g_m-V_{GS} @ #V_{DS}

New functionality: Inverter with same type of transistor possible





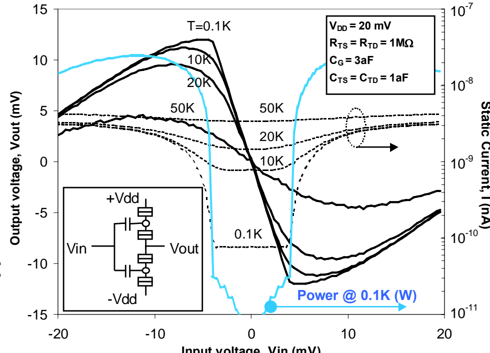
R_D # R_S but same capacitances: C_{TS}=C_{TD}

Digital SET ICs

- Almost all digital CMOS ICs can be replicated with SET but they lack current drive and speed!
- **SET inverter**
  - needs two identical SETs
  - power dissipation is essentially static:

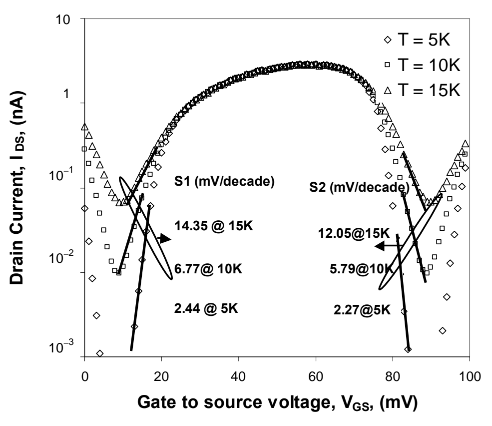
    Power ~ 10^{-8}-10^{-9} W

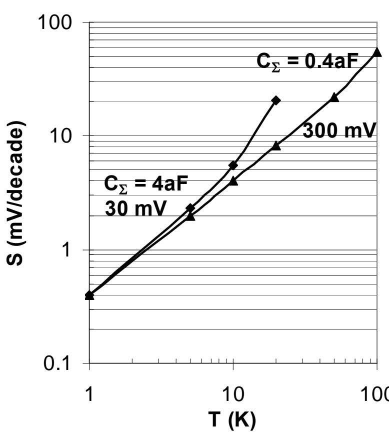
    4-5 decades lower than CMOS!
  - very sensitive to temperature: works under Coulomb Blockade



SET subthreshold slope

- not better than MOSFET @ room temperature
- not limited @ T < 20K



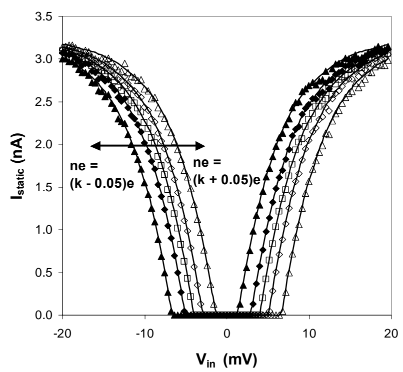


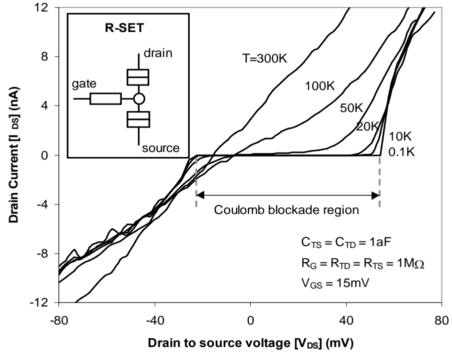
Background charge in SET

Effect of backgroud charge:
Significant shift of I_D-V_{GS}

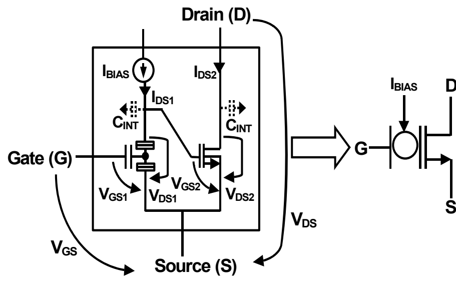
Solutions:

- device level: R-SET, SET with tuneable 2nd gate
- circuit level





SETMOS



SETMOS characteristics predicted by calibrated SPICE simulations: I_{peak} → μA!

Drain to Source Current, I_{DS} (μA)

Gate to Source Voltage, V_{GS} (V)

T = −100°C

I_{BIAS} = 40nA

V_{DS} (V) = 0.5, 0.4, 0.3, 0.2, 0.1

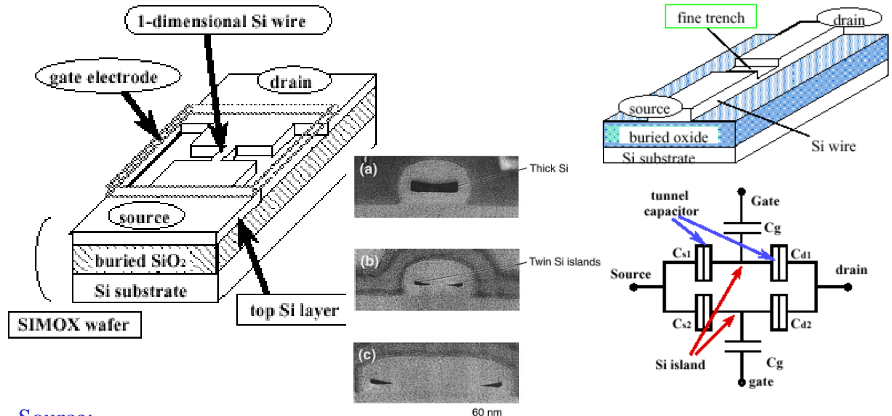
e/C_G = 0.8V

- constant current biased SET
- oscillations are transferred to the MOSFET gate voltage, biased in weak inversion: $I_D \sim \exp(qV_G/nkT)$
- needs hybrid CMOS/SET technology

Source:
S. Mahapatra & A. Ionescu, IEDM 2003, IEEE EDL 2004.

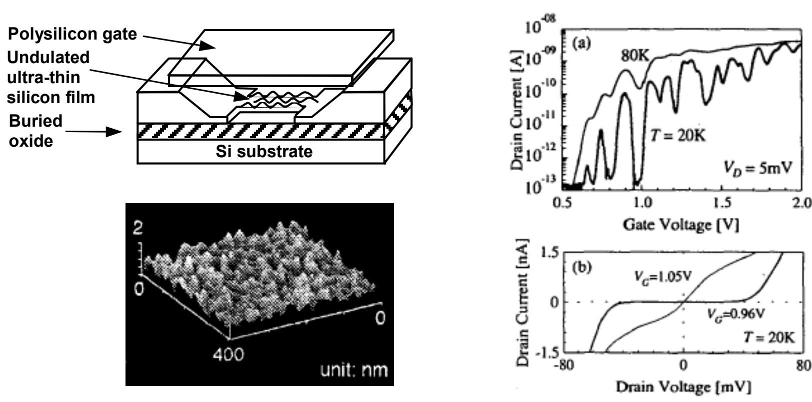
SET fabrication: PADOX and V-PADOX

(PAttern Dependent OXidation)



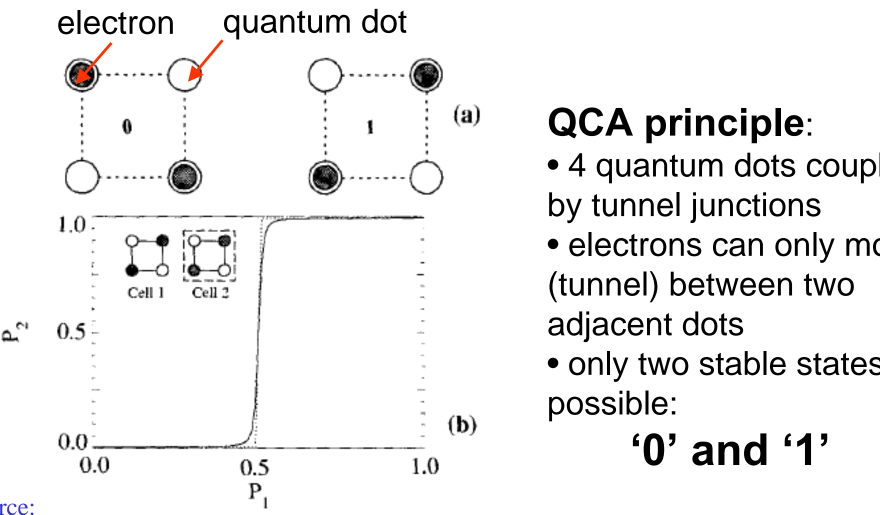
Source:
Y. Ono et al., IEEE Transactions on Electron Devices, Vol. 47, pp. 147 –153, January 2000.

SET fabrication: undulated SOI film



Source:
K. Uchida et al., Digest of 57th Annual Device Research Conference, pp. 138-139, June 1999.

Quantum Cellular Automata & wireless logic

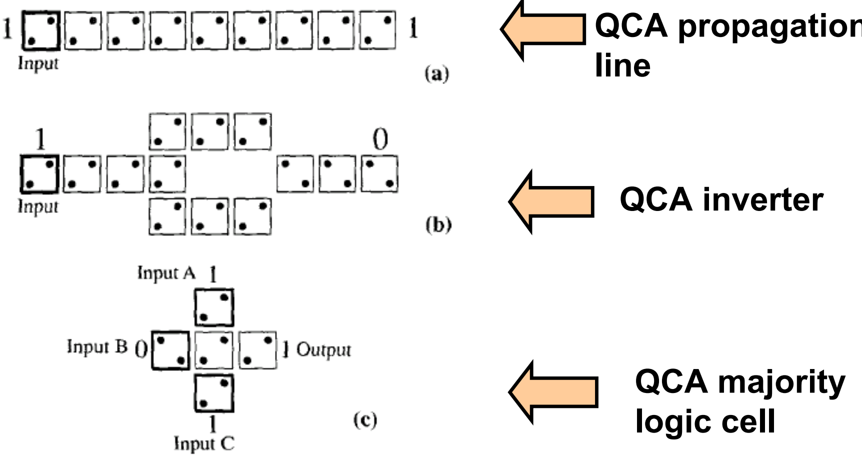


QCA principle:
- 4 quantum dots coupled by tunnel junctions
- electrons can only move (tunnel) between two adjacent dots
- only two stable states possible:

'0' and '1'

Source:
C. S. Lent and P. D. Tougaw, Proceedings of the IEEE, Vol. 85, pp. 541-557, April 1997.

Quantum Cellular Automata (1)



QCA propagation line

QCA inverter

QCA majority logic cell

Figure 2. (a) Line of QCA cells. (b) QCA inverter. (c) QCA majority gate.

Quantum Cellular Automata (2)

Experiment (G. Snider et al, University of Notre Dame)

→ quantum dots → **Al island** connected by **Al/AlOx/Al** tunnel junctions and **lithographically defined capacitors** (e-beam).

→ Works @ 70mK (thermal fluctuations are cancelled out)

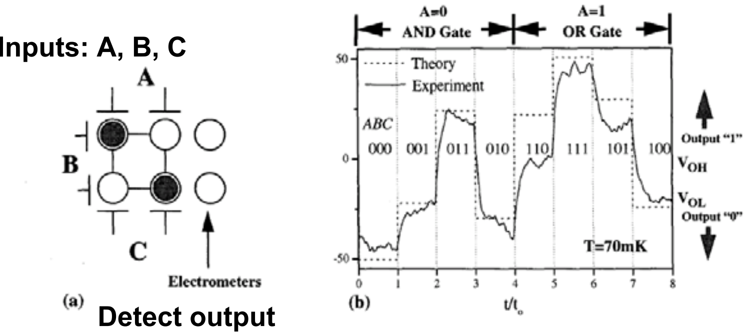


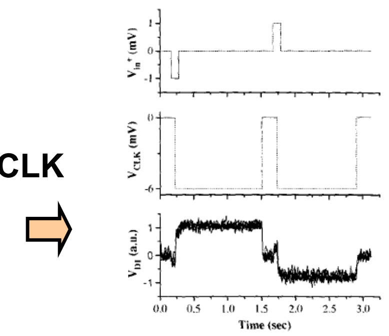
Figure 3. (a)Schematic diagram of QCA majority gate. (b) Measured output demonstrating AND/OR operation.

Quantum Cellular Automata (3)

Clocked QCA: nanowire microprocessor architecture

• **Clock** : mandatory for real applications
→ **enables (dictates) switching between successive states**
• **Quasi-adiabatic switching:** between system states the 'ground state' (equilibrium is maintained) → **control of tunneling (barrier) by a gate**

CLK



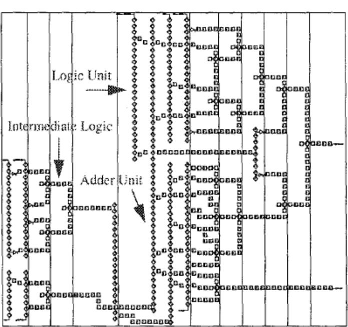


Fig. 5: 1st cut of the Simple 12 ALU

Quantum Cellular Automata (4)

Key advantages:
• Only the adjacent: **no need of long interconnects**
• The inputs & output placed exclusively at the periphery: **functionality defined by inter-cell propagation**
• computation corresponds to the **relaxation of the system toward a stable (equilibrium) state**
• Very small dimensions, highly compact**: dots < 20nm**
• Ultra low power consumption**: Power x delay ~ kT**

Issues:
• demonstrators only @ cryogenic temperatures : **T < 1K**
• **technology: not yet developed**
• intrinsic problem of **reverse propagation** (bi-directional) :
output → input (input → output)

Silicon Nanowires

Currently, there is intense interest in one-dimensional (1D) nanostructures, such as **nanowires (NWs)** and **nanotubes (NTs)**:

• due to their potential to test fundamental concepts about **how dimensionality and size affect physical properties**

• serve as **critical building blocks for emerging nanotechnologies**

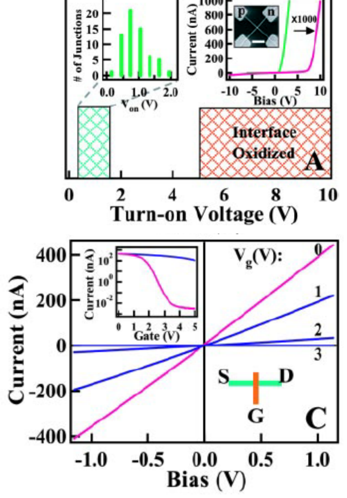
• enable **new integrated functionality in highly dense yet low cost integrated circuits**

Logic Gates and Computation from Assembled Nanowire Building Blocks (1)

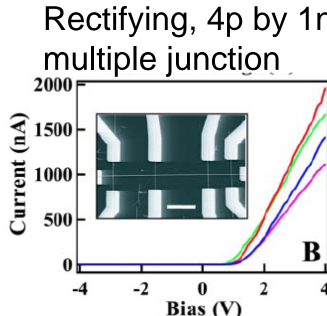
• **assembly of p-Si and n-GaN NWs (diameters: 10-25nm and 10-30nm, respectively)**
• crossed nanowire p(Si)-n(GaN) junctions and junction arrays to be assembled in over 95% yield with controllable electrical characteristics
• junctions can be used to create integrated nanoscale field-effect transistor arrays with nanowires as both the conducting channel and gate electrode
• in contrast with present nanotubes (NTs), **nanowires (NWs) can be assembled in a predictable manner**

Crossed NW nanodevice elements

Von of crossed NW junction



Rectifying, 4p by 1n multiple junction



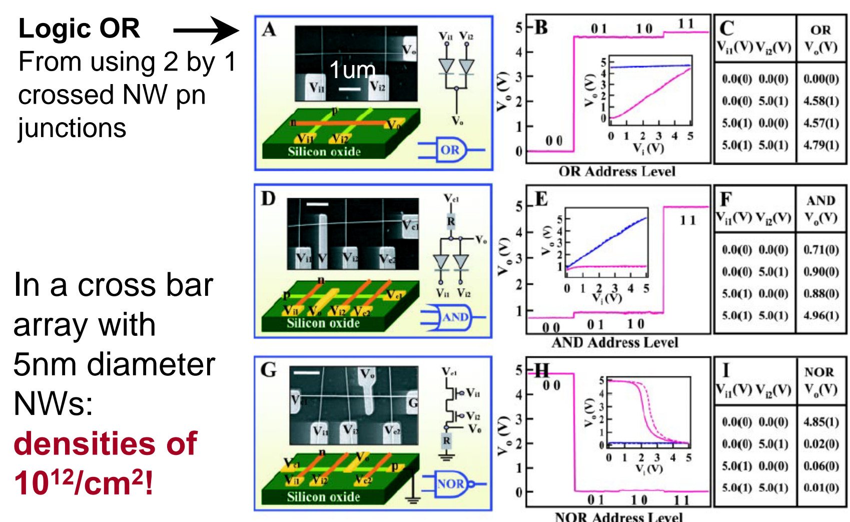
High turn-on junctions can be used as nano-scale FET (p-channel FET: cNW-FET), not a back gate solution

- oxide layer at the junction (thermal oxidation)

Nanowire logic gates

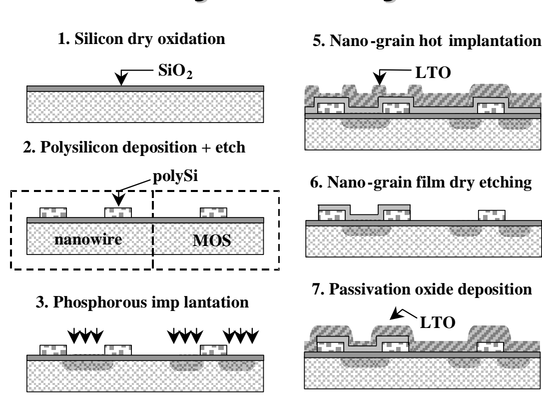
Logic OR →
From using 2 by 1 crossed NW pn junctions

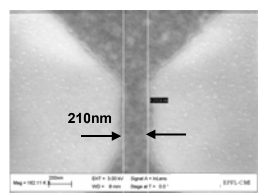
In a cross bar array with 5nm diameter NWs: **densities of $10^{12}/cm^2$!**



Source: Y. Huang et al., Science, Vol. 294, pp. 1313–1317, 2001.

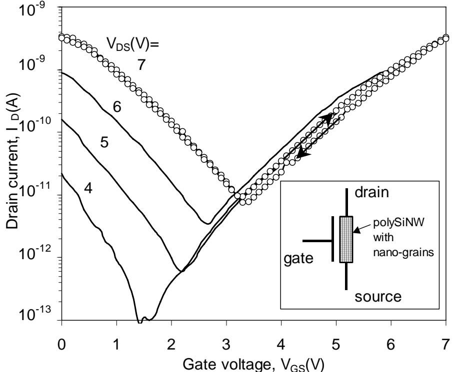
Hybrid Poly-SiNWs/CMOS





- Ultra-thin film polySi NW with nanograins (5-20nm)
- Highly P-doped ($10^{19}cm^{-3}$)
- In-NMOS process

I-V characteristics and bias scheme of Poly-SiNWs



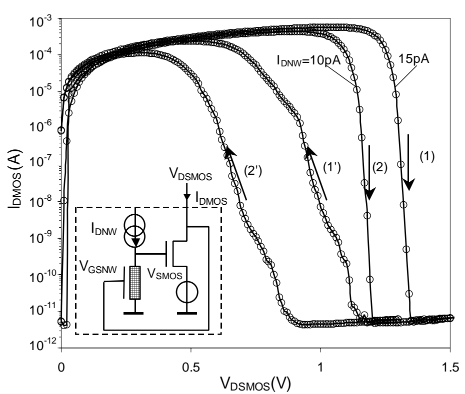
V-shaped (log scale) characteristics and hysteresis of polySiNW.

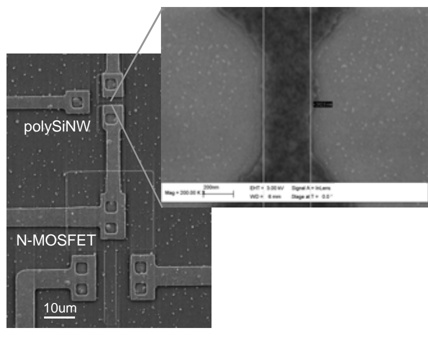
Drain voltage, V_{DS} (V)
I_D
V_{GS}
V_{DS}
I_D=20pA
ΔI_D=5pA
5pA
Gate voltage, V_{GS} (V)

V_{DS}-V_{GS} transfer characteristics of polySiNW at constant current.

Source: S. Ecoffey et al., ISSCC 2005.

Hybrid polySiNW-MOS NDR cell



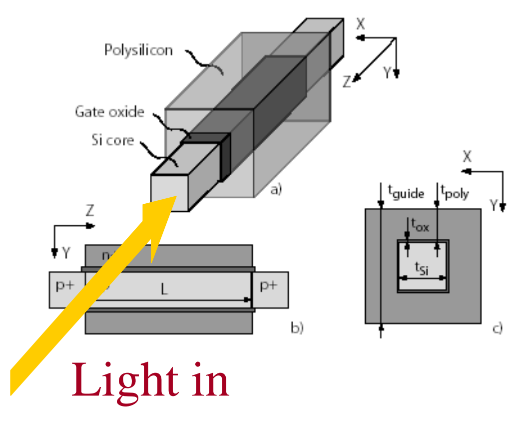


Hybrid polySiNW-MOS Negative differential Resistor with record characteristics @ room temperature:

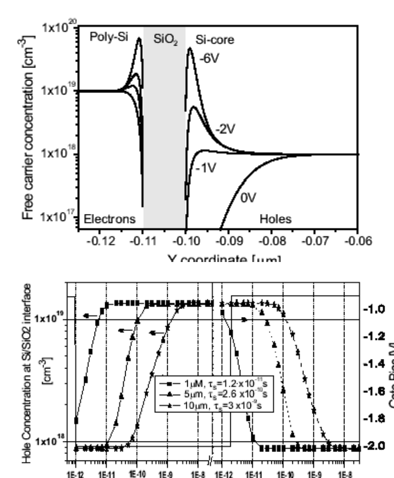
- Ipeak/Ivalley ~ 8 decades
- Subthreshold slope: -10mV/decade

Nanowires for integrated optoelectronics

Gate-All-Around SOI NW modulator



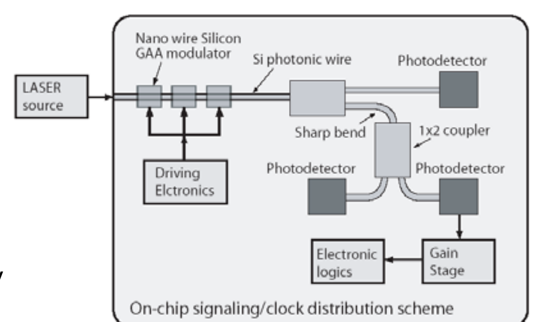
K. Moselund, P.Dainesi, A.M. Ionescu, Transducers 2005.



SOI NW on-chip optical interconnects for clock distribution

Advantages

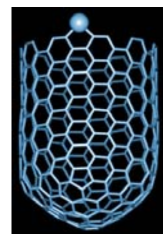
- Propagation of light signals independent of modulation frequency
- Precise, synchronous clock distribution
- Voltage isolation – optical detectors count photons



Challenges:

- Scalability: size and frequency
- Integration of photodetector @ infrared wavelenghs on Si
- Integration with CMOS
- Si light-source on-chip?

Carbon Nanotube (1)



• CNT is a **tubular form of carbon with diameter ~1 nm** and length **~ few nm to microns**.
• CNT is configurationally equivalent to a two dimensional graphene sheet rolled into a tube.

• STRIP OF A GRAPHENE SHEET ROLLED INTO A TUBE
(n,0) / ZIG ZAG
(m,m) / ARM CHAIR
CHIRAL (m,n)

• CNT has extraordinary mechanical properties: **Young's modulus over 1 Terra Pascal, as stiff as diamond**, and tensile strength ~ 200 GPa.
• CNT can be **metallic or semiconducting**, depending on chirality
• Thermal conductivity ~ 3000 W/mK in the axial direction with small values in the radial direction

Carbon Nanotube (2)

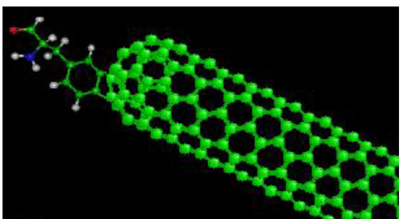
- **Electrical conductivity up to orders of magnitude higher than copper**

- Can be metallic or semiconducting depending on chirality
  - **tunable bandgap**
  - electronic properties can be tailored through application of external magnetic field or mechanical deformation

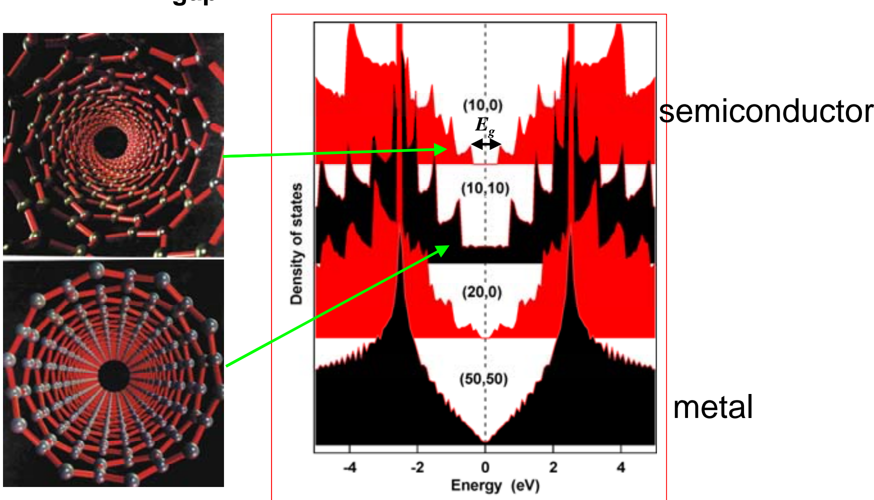
- Very **high current carrying capacity**

- **Excellent field emitter**; high aspect ratio and small tip radius of curvature are ideal for field emission

- Can be functionalized

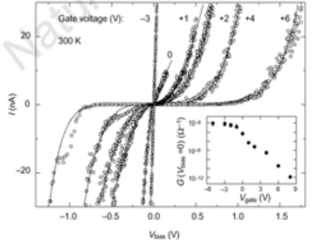


Electronic structure of SWCNT
E_{gap} scales as 1/diameter

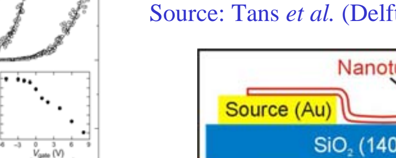


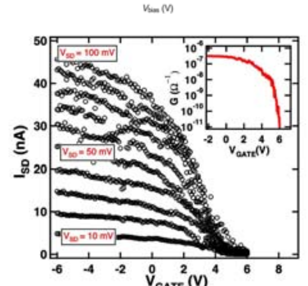
Source: R. Martel, DAC 2002.

1998 : First Carbon Nanotube Field Effect Transistor



Source: Tans *et al.* (Delft) Nature **393**, 49 (1998)

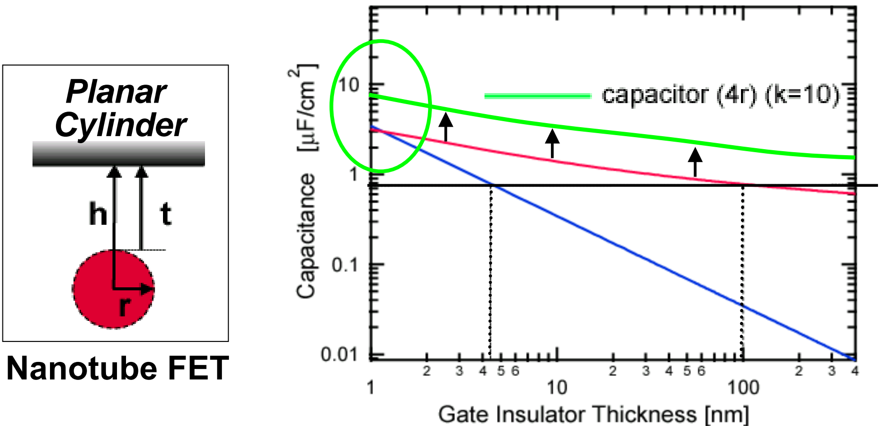




Source: Martel *et al.* (IBM), App. Phys. Lett. 73, 2447 (1998)

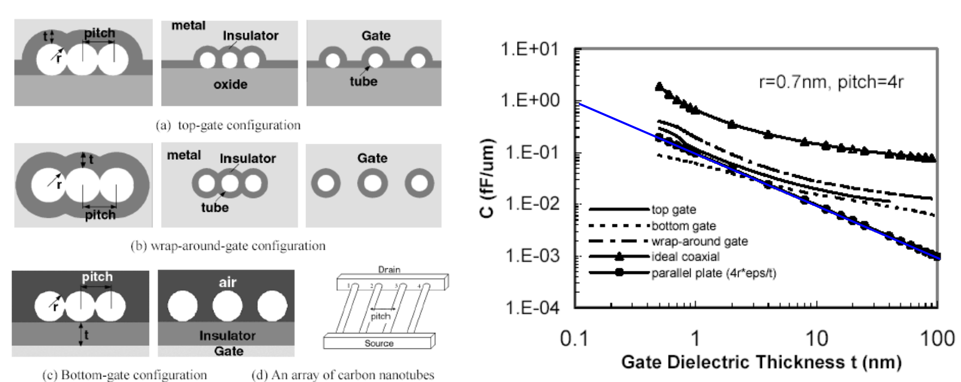
- P-type
- High contact resistance
- Hole mobility ~ $20 cm^2/Vs$

CNT: gate capacitance scaling issues



C ~ 1/t (plate) → C~ 1/ln(2h/r) (cylinder)

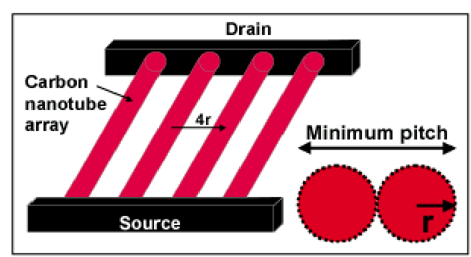
CNT: gate capacitance scaling issues



Source:
X. Wang et al., SISPAD 2003, Sept. 2003, pp.163-166.

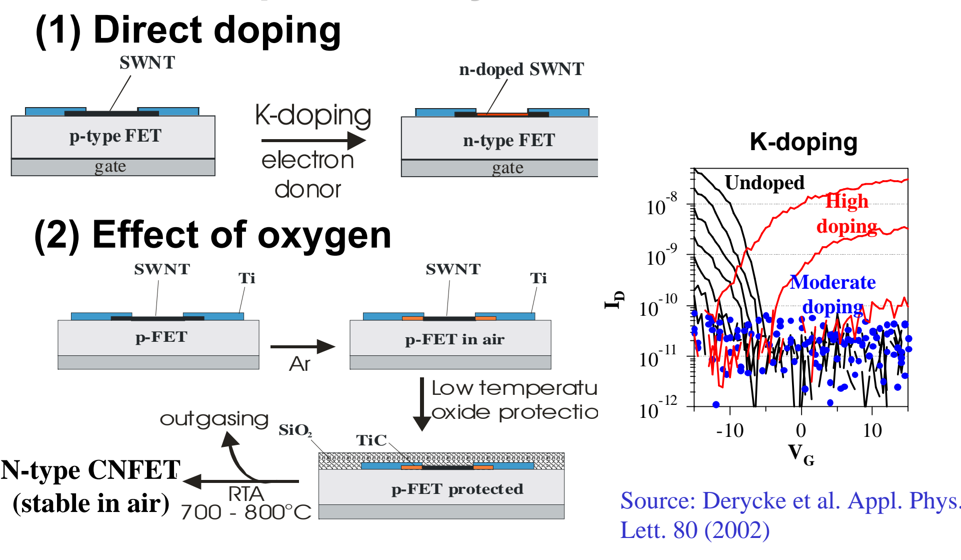
Carbon Nanotube FET versus Si FET

Array with 4r



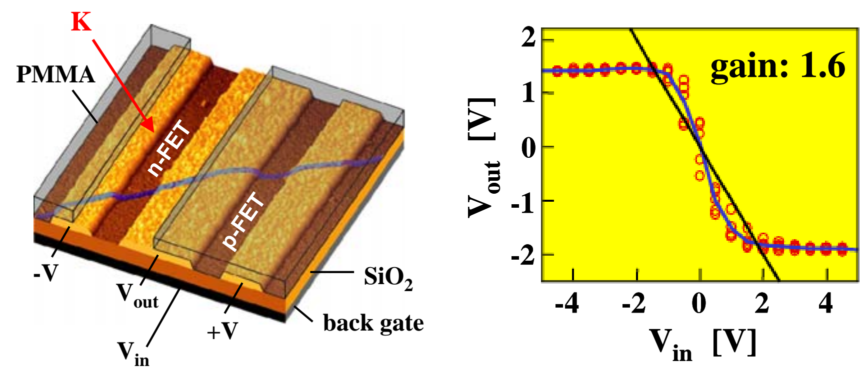
Transistor	p-CNFET 300 nm (Co)	Si MOSFET 100nm	Si MOSFET 25nm
Transconductance (µS/µm)	(3 µS/tube) 1160	1000 (nFET) 460 (pFET)	1200 (nFET) 640 (pFET)
External resistance (Ω-µm per side)	<100	~66 (nFET) ~143 (pFET)	~40 (nFET) ~86 (pFET)
"Field Mobility" (cm^{2}V^{-1}s^{-1})	>70 ?	~50-160	------
Gate insulator(nm)	15	2.0	0.8

Complementary nanotube FET



Source: Derycke et al. Appl. Phys. Lett. 80 (2002)

CNT inverter

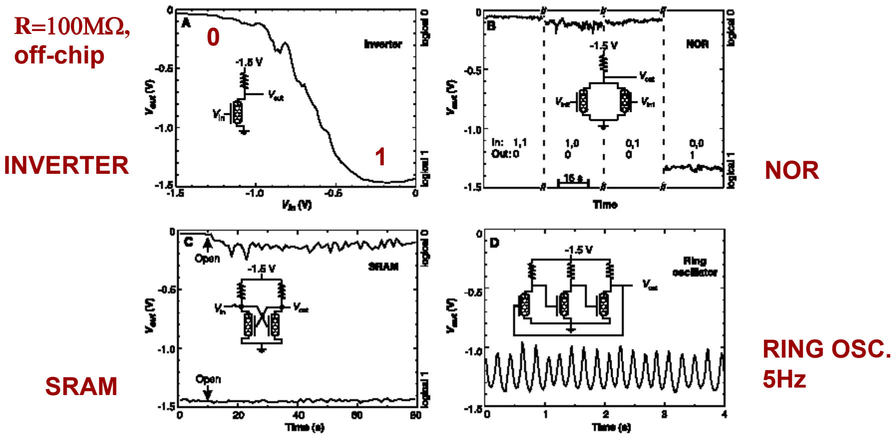


Source: Derycke et al. Nano Letters 1(9), 453 (2001)

Basic IC functionality demonstrated with SW CNTs

R=100MΩ,
off-chip

INVERTER



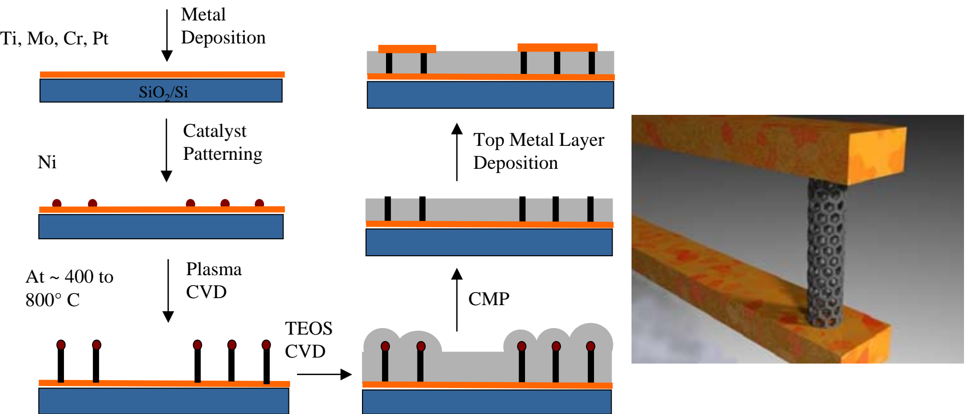
NOR

SRAM

RING OSC.
5Hz

Source:
A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker, Science, Volume: 294, pp. 1317-1320, 2001.

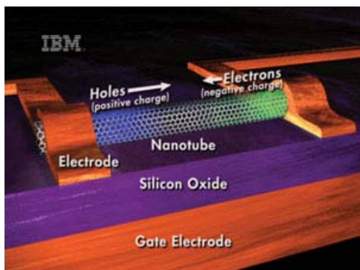
Bottom-up Approach for CNT Interconnects

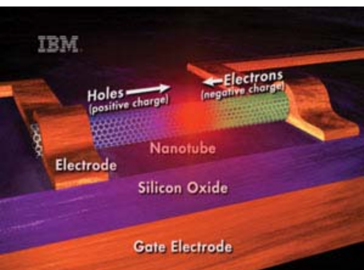


Source: J. Li, Q. Ye, A. Cassell, H. T. Ng, R. Stevens, J. Han, M. Meyyappan, *Appl. Phys. Lett*., **82**(15), 2491 (2003)

Carbon nanotubes as light emitters

Potential to be built in arrays or integrated with carbon nanotube or silicon electronic components, opening new possibilities in electronics and optoelectronics





Polarized infrared optical emission observed from SWCNT ambipolar FET

Source: IBM, J.A. Misewich, R. Martel, Ph. Avouris, J.C. Tsang, S. Heinze, and J. Tersoff, Science, May 2, 2004.

Carbon nanotubes as Nano-Electro-Mechanical devices

Nanorelay

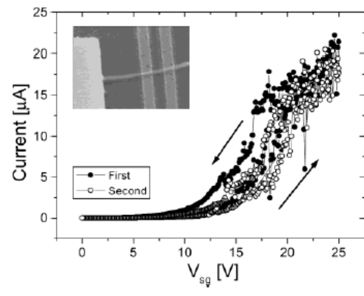
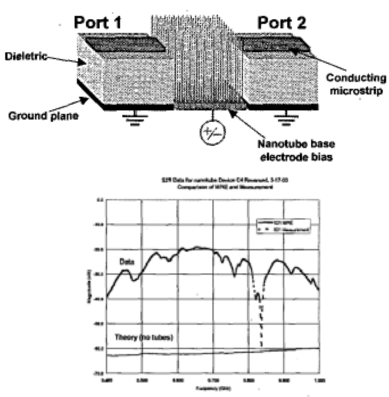


Figure 3. $I-V_{sg}$ characteristics of a nanotube relay initially suspended approximately 80 nm above the gate and drain electrodes. Current increased nonlinearly as the gate voltage increased (V_g < 20 V). Linear current increase and strong fluctuations are seen for V_{sg} > 20 V. The source−drain voltage, V_{sd}, was 0.5 V.

Source: S. Lee et al., Nanoletters, 2004.

Nanoresonator array



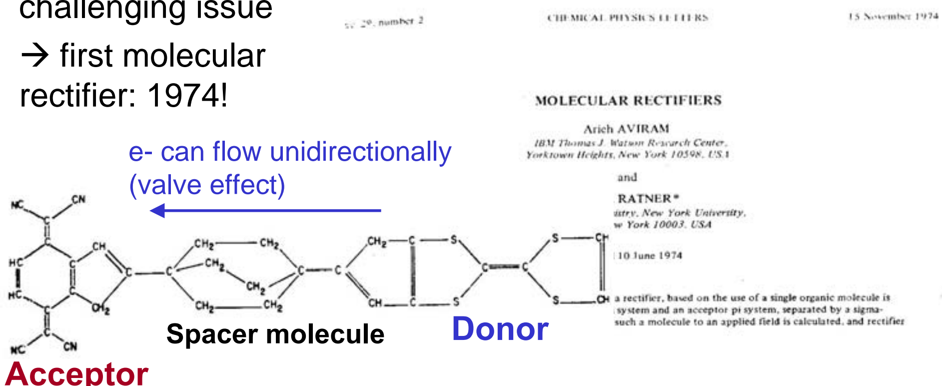
Source: J.F. Davis et al., Nanotechnology, 2003.

Molecular Electronics

• The purpose of molecular electronic is to **reduce the size or electronic devices to that of a single molecules**

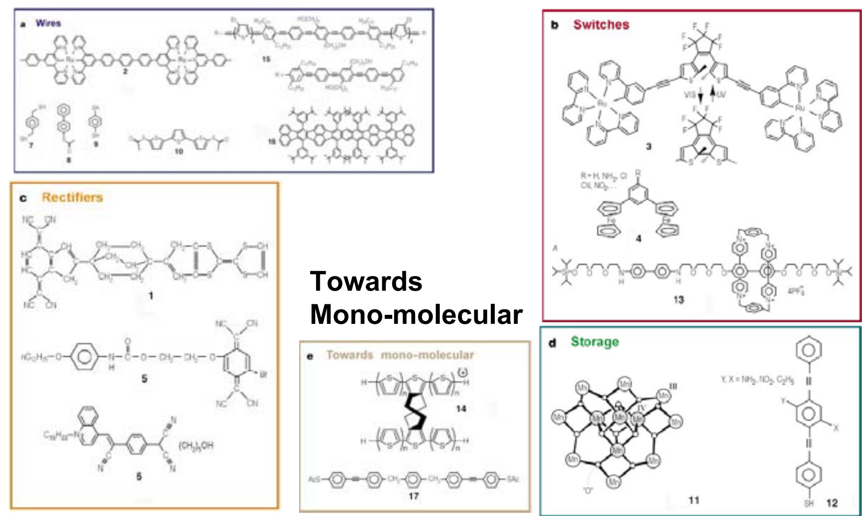
• **Connecting a molecule** to the external world is still a challenging issue

→ first molecular rectifier: 1974!

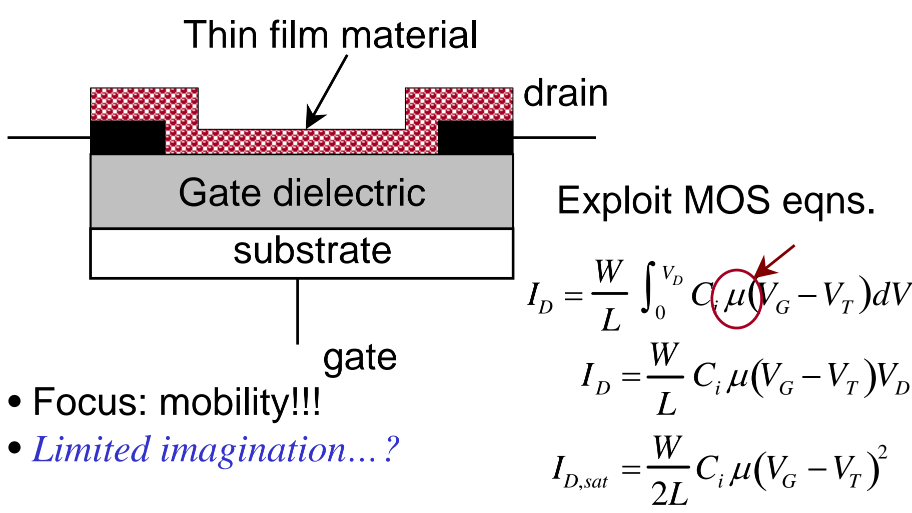


Electrical addressing of molecules

molecules for # functionalities!



Test vehicle for molecular conduction: thin-film field effect transistor



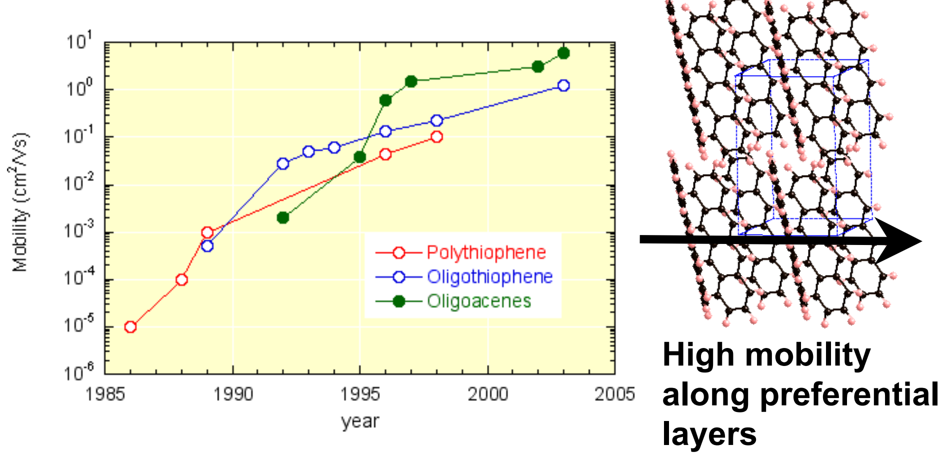
$$I_D = \frac{W}{L}\int_0^{V_D} C_i \mu (V_G - V_T) dV$$

$$I_D = \frac{W}{L} C_i \mu (V_G - V_T) V_D$$

$$I_{D,sat} = \frac{W}{2L} C_i \mu (V_G - V_T)^2$$

- Focus: mobility!!!
- *Limited imagination…?*

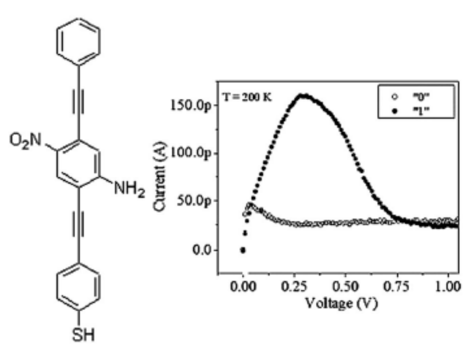
Carrier mobility in categories of molecular materials



Charge transport in organic semiconductors

- **Delocalized transport (diffusion limited)**
  - Mean free path > de Broglie wavelength
  - Mobility **decreases when temperature increases**
- **Hopping (localized) transport**
  - $\mu < 0.01$ cm^2/Vs
  - Mobility is **thermally activated**
- **Current performance**
  - $\mu > 1$ cm^2/Vs still low

Working example: NDR molecular device



- switch based on phenylene ethynylene molecules
- 10^9 cycles without degradation of I-V
- logic possible using NDR

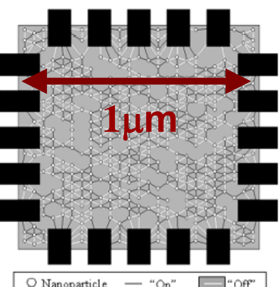


Fig. 2. Shown is our first experimentally obtained $I(V)$ curve of a self-assembled monolayer of 1 between two metallic contacts [11], [12]. Initially, the $I(V)$ response is in the "0" state (open circles). Once application of a 1.75-V pulse takes place, the molecule sets into a new state, "1" (black circles), that exhibits NDR behavior wherein the current rises then falls with increased voltage. Initial simulations used this $I(V)$ curve.

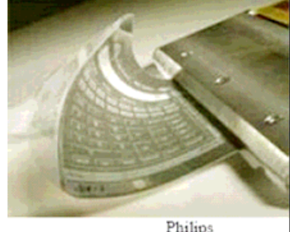
Source:
J. M. Tour et al., IEEE Transactions on Nanotechnology, Vol. 1, pp. 100-109, June 2002.

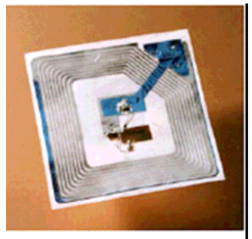
Why organic semiconductors?

Large area, low cost flexible electronics!

Applications: electronic book, electronic paper, RF-ID tags, sensors, flexible solar cells

Lucent/E-Ink


Philips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Spintronics

What is Spintronics?

• New technoogical and nanoelectronic discipline which aims to exploit the subtle esoteric quantum properties of the electron to develop a new generation of electronic devices.

• It ***exploits the SPIN of the electron***: the electron has an intrinsic angular momentum with a spin value of 1/2 and the spin can be in two states: ***spin-up*** and ***spin-down***.

• Electron's magnetic momentum is proportional to its spin: ***spintronics is intrinsincally linked to magnetism***.

Magnetoelectronics

• spin of electrons is important
• Normal metals, like **aluminum or copper, are spin compensated and non-magnetic**. Their electron spin is irrelevant.
• **Net spins do exist in magnetic metals, like iron or cobalt,** which are essential to materials for magnetoelectronics. This is not predictable by classical physics but by quantum mechanics:

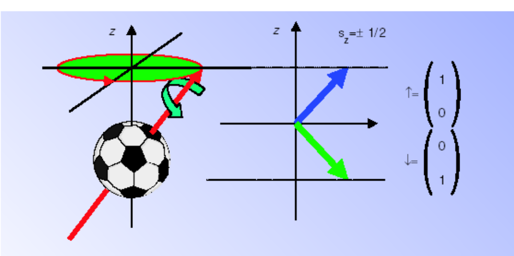


Fig. 1 An electron and its quantized spin (enlarged)

Model:
Spining soccer ball that precesses (a gyration of the rotation axis of spinning body about another line intersecting it) such that only the component along a spin-quantization axis (here paralle to z) is fixed.

Giant Magnetoresitive Effect (GMR)

• discovered in 1988 by Albert Fert's group in France
• observed in artificial thin-film materials composed of alternate ferromagnetic and non-magnetic layers:
(i) **RESISTANCE of the material is the LOWEST when the magnetic moments of the ferromagnetic materials are ALIGNED**
(ii) **RESISTANCE of the material is the HIGHEST when the magnetic moments of the ferromagnetic materials are ANTIaligned**
• **The current can be both PERPENDICULAR or PARALLEL to the interfaces**

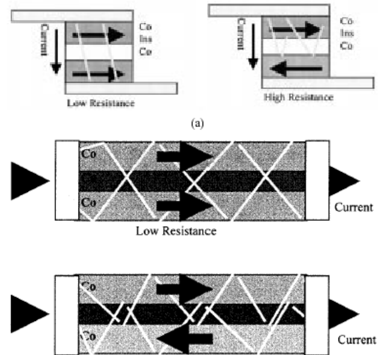
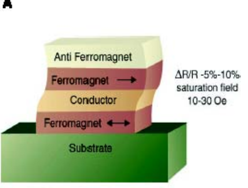


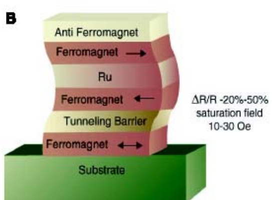
Fig. 2. Comparison of spintronic devices where current is (a) Perpendicular to the Plane (CPP) and (b) Current is In-Plane (CIP).

Spin-based devices

• **Spin-valve**:
A GMR-based device with two ferromagnetic layers (alloys of nickel, iron, cobalt) sandwitching a thin non-magnetic layer (copper), with one of the two magnetics layers pinned (magnetization insensitive to moderate magnetic fields). Pinning is accomplished by using an antiferromagnetic layer in intimate contact with the pinned magnetic layer. Change in resistance: 5-10%.

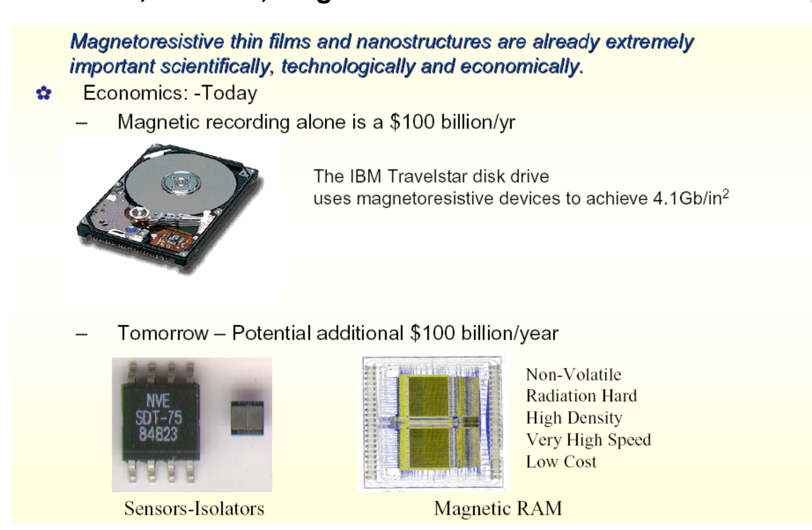


• **Magnetic tunneling junction**:
A device in which a pinned layer and a magnetic layer are separated by a very thin insulating layer (Al2O3). The tunneling resistance is modulated by the magnetic field in the same way as the resistance of spin-valve, exhibiting **20-40%** in magneto-resistance.

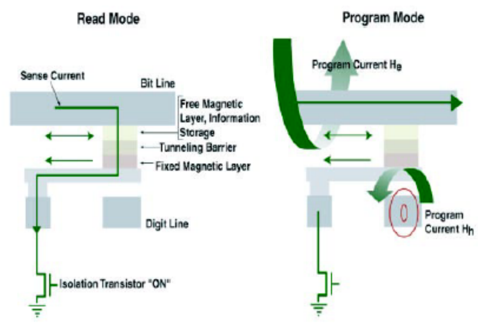


Applications of GMR devices:

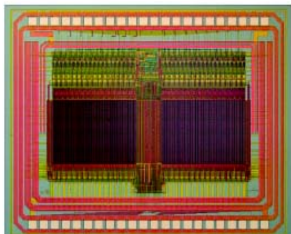
hard drives, sensors, magnetoresistive random access memory



MTJ application in commercial MRAM



1T1MTJ MRAM cell (Motorola)



256kB MRAM chip

SPIN INJECTION in a semiconductor

To make new spintronic components research has to address 3 problems:

(1) **Creation of a spin-ensemble in a semiconductor**

(2) **External control over spin-packet movement** (co-herence and lifetime on a sub-micron scale in a frame time of nano to micro-seconds

(3) External observation: **READ of spintronic device function**

CONCLUSION
To More Moore and… After

• Main applications of any sufficiently new and innovative technology always have been – and will continue to be – **applications CREATED by that new technology**

• People should remember the fact that DISCOVERY **does not work by DECIDING** what you want and **THEN DISCOVERING IT**

Source: Herbert Kroemer (Nobel Prize)

Industry research: large CMOS pizza!

Academic research (nanowires, nanotubes, nanodots…) : French cuisine!